REMARKS

The foregoing amendment is provided to impart greater clarity to and to more particularly point out the claimed invention and to place the current application in condition for allowance, rather than to avoid prior art.

Applicant respectfully requests reconsideration of the above identified application. Claims 1-25 are pending. Claims 1-3, 6, 7, 16-20, 24 and 25 are rejected. Claim 25 is amended. Claims 26-33 are added.

Applicant respectfully notes that in the Office Action mailed on May 25, 2005, interpretations or characterizations by the Examiner include inferences and/or potential limitations, to which Applicant does not agree. Being respectful of the Examiner's time, Applicant will address only the issues necessary to traverse the rejections, but reserves the right to refute such interpretations or characterizations at a later time if necessary.

The remaining comments are directed to Claims 1-33.

35 U.S.C. § 102 REJECTIONS

The Office Action mailed on May 25, 2005 rejects Claims 1-3, 6-7, and 25 under 35 U.S.C. 102(e) as allegedly being anticipated by US Pat. No. 6,762,964 (Takase).

Claim 1, for example, sets forth an apparatus comprising:

a bit vector replacement circuit to receive a first bit vector and a control signal and to substitute a constant bit vector for the first bit vector, in response to the control signal being in a first state, to produce a second bit vector;

a pre-decoder coupled with the bit vector replacement circuit to receive a plurality

of bit vectors including the second bit vector, to combine subsequences from the plurality of bit vectors to identify possible wordline subsequences corresponding to the plurality of bit vectors, and to activate a subsequence indicator for an identified possible wordline subsequence; and

a wordline decoder coupled with the pre-decoder to combine activated subsequence indicators to identify a unique wordline corresponding to the plurality of bit vectors.

To anticipate a claim, a prior art reference must disclose every limitation of the claimed invention, either explicitly or inherently. In re Schreiber, 128 F.3d 1473, 1477, 44 USPQ2d 1429, 1431 (Fed. Cir. 1997).

Takase, Applicant respectfully submits, discloses that decoder 506 activates a replacement control signal line for a defective column address and a spare column select line (col. 7, lines 45-64; 4 of Fig. 4; 4 and 9_i of Fig. 1) but decoder 506 does not to identify possible wordline subsequences and activate a subsequence indicator for an identified possible wordline subsequence as claimed. Takase discloses that wordlines and rows are equivalent (col. 4, lines 37-64; Fig. 1; 3 of Fig. 2) and that in each row, there is a spare column (col. 5, lines 8-12; SCSL of Fig. 2). The wordline decoding (row decoding) of Takase is remarkably uninteresting, to the extent that Takase finds no need to describe it in detail (col. 4, lines 53-55; 3 of Fig. 1 and 3 of Fig. 2). Takase does not disclose or suggest a wordline decoder coupled with the pre-decoder to combine activated subsequence indicators to identify a unique wordline as claimed.

Therefore, Applicant respectfully submits that not every limitation of the claimed invention, is disclosed either explicitly or inherently by Takase.

Similarly, Claim 25 as amended sets forth a method comprising:

copying a plurality of storage locations from a second storage into a plurality of wordlines of the first storage by asserting corresponding wordline signals;

receiving an access request including a first bit vector, a second bit vector and a control signal;

setting the second bit vector equal to a constant bit vector if the control signal is in a first state;

identifying at least in part from the second bit vector and from the first bit vector a wordline corresponding to the combined first bit vector and second bit vector;

asserting the identified wordline signal; and

accessing the wordline of the first storage corresponding to the asserted wordline signal.

As discussed above Takase activates a replacement control signal line for a defective column address and a spare column select line (col. 7, lines 45-64; 4 of Fig. 4; 4 and 9_i of Fig. 1) but does not use the replacement control signal lines to identify a wordline. Therefore, Applicant respectfully submits that not every limitation of the claimed invention, is disclosed either explicitly or inherently by Takase.

Accordingly in light of the argument presented above, Applicant respectfully requests the Examiner withdraw the rejection of Claims 1-3, 6-7, and 25 for allegedly being anticipated by Takase.

The Office Action rejects Claim 24 under 35 U.S.C. 102(e) as allegedly being anticipated by US Pat. No. 5,835,928 (Auslander).

Claim 24 sets forth a cache memory system comprising:

a plurality of lines for storing copies of memory storage locations having corresponding addresses;

means for decoding an address to access a line of the cache memory system responsive to an access request that includes an address represented in a redundant form; and

means for decoding an address to access a line of the cache memory system

responsive to an access request that includes an address represented in unsigned binary form.

Auslander, Applicant respectfully submits, discloses that a CAM matches multi-bit binary addresses with multi-bit binary addresses previously stored and asserts a common match line 22 if the input binary address matches a previously stored binary address (col. 5, lines 9-18) but does not disclose an access request that includes an address represented in a redundant form as claimed. Therefore, Applicant respectfully submits that not every limitation of the claimed invention, is disclosed either explicitly or inherently by Auslander.

Accordingly in light of the argument presented above, Applicant respectfully requests the Examiner withdraw the rejection of Claim 24 for allegedly being anticipated by Auslander.

35 U.S.C. § 103 REJECTIONS

The Office Action mailed on May 25, 2005 rejects Claims 16-18 under 35 U.S.C. 103(a) as allegedly being unpatentable over US Pat. No. 6,762,964 (Takase) and Claims 19-20 as allegedly being unpatentable over Takase, and in view of US Pat. No. 6,317,810 (Lopez-Aguado).

Claim 19 sets forth a digital computing system comprising:

a die;

a bit vector selection circuit on the die to receive a first bit vector and a control signal, and to select a constant bit vector or the first bit vector responsive to the control signal, and to output the selected bit vector as a second bit vector;

a decoder circuit on the die coupled to the bit vector selection circuit to receive a plurality of bit vectors including the second bit vector and to combine a subsequence from each of the plurality of bit vectors to identify a wordline corresponding to the

plurality of bit vectors;

an internal cache on the die, the internal cache coupled with the decoder circuit to store a first datum at the wordline corresponding to the plurality of bit vectors;

a processor on the die coupled with the decoder circuit to produce the plurality of bit vectors; and

an external cache, not on the die, to store a second datum, the external cache coupled with the die and with the internal cache, to transmit the second datum to the internal cache to be stored on the die.

As discussed above with respect to Claim 1, The wordline decoding (row decoding) of Takase is remarkably uninteresting (col. 4, lines 53-55; 3 of Fig. 1 and 3 of Fig. 2). Applicant respectfully submits, that decoder 3 does not combine a subsequence from each of the plurality of bit vectors to identify a wordline as claimed.. Applicant also respectfully submits, that decoder 506 activates a replacement control signal line for a defective column address and a spare column select line (col. 7, lines 45-64; 4 of Fig. 4; 4 and 9_i of Fig. 1) but decoder 506 does not combine a subsequence from each of the plurality of bit vectors to identify a wordline as claimed.

Therefore, Applicant respectfully submits that not every limitation of the claimed invention, is disclosed or made obvious by Takase and/or Lopez-Aguado.

Accordingly, Applicant respectfully requests the Examiner withdraw the rejection of Claim 19 for allegedly being unpatentable over Takase and in view of Lopez-Aguado.

Therefore, Applicant respectfully submits that Claims 1, 19, 24 and 25 are patently distinguished over the art cited by the Examiner. Applicants further believe that Claims 2-18 and 20-23 and newly added Claims 26-33, being dependent therefrom are also patentable.

Applicants, therefore, believe that Claims 1-33 are presently in condition for allowance and such action is earnestly solicited.

CONCLUSION

Applicants respectfully submit the present claims for allowance. If the Examiner believes a telephone conference would expedite or assist in the allowance of the present application, the Examiner is invited to call Lawrence M. Mennemeier at (408) 765-2194.

Authorization is hereby given to charge our Deposit Account No. 02-2666 for any charges that may be due.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN

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